L Number	Hits	Search Text	DB	Time stamp
1	2	("6011710").PN.	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:28
2	2	("6002632").PN.	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:29
3	4498	(memory adj controller) and host	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:30
4	1726	((memory adj controller) and host) and (data adj bus)	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:30
5	819	(((memory adj controller) and host) and (data adj bus)) and switch	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:31
6	2	((((memory adj controller) and host) and (data adj bus)) and switch) and (parasitic adj capacitance)	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:32
7	5	((((memory adj controller) and host) and (data adj bus)) and switch) and parasitic	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:33
8	791	((((memory adj controller) and host) and (data adj bus)) and switch) and access	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:33
9	695	(((((memory adj controller) and host) and (data adj bus)) and switch) and access) and processor	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:36
10	224	((((((memory adj controller) and host) and (data adj bus)) and switch) and access) and processor) and (host adj processor)	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:36
11	157	(((((((memory adj controller) and host) and (data adj bus)) and switch) and access) and processor) and (host adj processor)) and DRAM	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:37
12	128	(((((((memory adj controller) and host) and (data adj bus)) and switch) and access) and processor) and (host adj processor)) and DRAM) and synchronous	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:37
13	58	(((((((((memory adj controller) and host) and (data adj bus)) and switch) and access) and processor) and (host adj processor)) and DRAM) and synchronous) and coupling	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:50
14	4	((((((memory adj controller) and host) and (data adj bus)) and switch) and access) and processor) and (365/63.ccls.)	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 14:52
15	33	(((memory adj controller) and host) and (data adj bus)) and (365/230.03.ccls.)	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 15:10
16	256	((((memory adj controller) and host) and (data adj bus)) and switch) and (chip adj select)	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 15:10
17	186	(((((memory adj controller) and host) and (data adj bus)) and switch) and (chip adj select)) and multiplexer	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 15:11

18	98	((((((memory adj controller) and host) and (data adj bus)) and switch) and (chip adj select)) and multiplexer) and coupling	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 15:11
19	98	(((((((memory adj controller) and host) and (data adj bus)) and switch) and (chip adj select)) and multiplexer) and coupling) and access	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 15:11
20	82	((((((((memory adj controller) and host) and (data adj bus)) and switch) and (chip adj select)) and multiplexer) and coupling) and access) and DRAM	USPAT; EPO; JPO; DERWENT; USOCR	2003/04/17 15:11